Wireless Integrated Circuit for the Acquisition of Electrocorticogram Signals

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***Abstract*—We present the design and characterization of amplifiers and control logic for an integrated circuit designed to record electrocorticograms (ECoG) from the surface of the brain. The chip, which was fabricated in a 0.6-µm BiCMOS process, contains 100 amplifiers, control logic, and circuits for wireless power and transmission of data. ECoG signals, sensed by electrodes, are capacitively coupled to the amplifiers. Each amplifier has a gain of 59.2 dB, a maximum bandwidth of 240 Hz, an input referred noise of 2.8 µV, and consumes 4.5 µW of power. The output of each amplifier is connected to a 10-bit ADC via an adaptive-bias buffer and transmission gate whose transparency is set by the control logic. The control logic time-shares the ADC by multiplexing through one of five preset patterns of 32 on-chip signals. The digitized waveforms are then broadcasted wirelessly using a 900 MHz FSK transmitter. The entire chip consumes 7.2 mW of power during operation.**

I. Introduction

Traditionally, electrocorticograms (ECoGs) have been used to locate the focus of epileptic seizures in the brain. If the focus is in an operable spot then surgical removal of that portion of the brain often eliminates seizures. ECoG signals are recorded by placing electrodes directly on the surface of the brain, on top of or underneath the thin dura mater that surrounds the brain. Before the brain can be mapped, a patient must undergo surgery to place the electrodes on the brain. Transcutaneous wires are connected to amplifiers and recording equipment, leaving the patient bound to a bed for several days until a sufficient number seizures have been recorded to accurately pinpoint their focus. A wireless ECoG recording device could free the patient from the confinement of the wires during the time between operations and greatly reduce the risk of infection.

A wireless device to record ECoG signals could also be used in a brain-machine interface (BMI). BMIs record neural signals and process them to control prosthetic devices. Due to the low fidelity of neural activity recorded outside the body, electroencephalograms (EEG) have limited usefulness as signals for next-generation BMIs. ECoG signals have higher amplitudes, wider bandwidth, and higher spatial resolution than EEGs as they have not been attenuated and dispersed through the skull and scalp. A recent study shows that the spatial resolution of ECoG is denser than previously thought, making this neural signal promising for improved BMIs [1].

In this paper, we present experimental results from a fabricated ECoG recording chip, designated INI-E: Integrated Neural Interface, ECoG. Fig. 1 shows a block diagram of the chip; Fig. 2 shows a die photo. INI-E is based on wireless technology previously developed for recording the activity of single neurons [2]. Previously-developed subsystems include circuits for receiving commands and power through an inductive link, as well as an ADC and RF transmitter to digitize the recorded data and broadcast it off chip. This paper focuses on the development of novel amplifiers optimized for ECoG signals, and control circuitry to export the recorded data from multiple electrodes, as well as characterization and testing of these circuits.

II. INI-E System Design

A. Amplifier Design

A schematic of the ECoG amplifier is shown in Fig. 3. Capacitors block the dc offset present at the electrode-tissue interface that would otherwise saturate the amplifier. The operational transconductance amplifiers (OTAs) are designed for low-noise, low-power operation using the techniques outlined in [3].

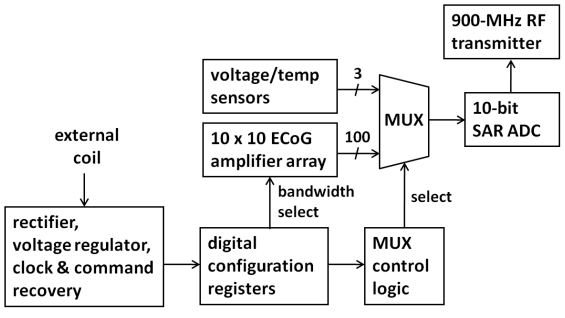

Figure 1. Block diagram of ECoG recording chip.

The first two stages of the ECoG amplifier provide a total of 60 dB of gain. To minimize noise, it is best to allocate more gain in the first stage. However, as the gain increases in the first stage, the size of C_1 also increases. Thus, there is a trade-off between low noise and layout area (and input impedance) in choosing the optimal gain for the stages. The gain of each stage was chosen so that the capacitors of each stage would have reasonable values while providing reasonable electrode-referred noise. The first stage provides 40 dB of gain and the second stage provides the remaining 20 dB. The OTAs for the first two stages need to have low offset voltages and low power consumption. As they drive capacitive loads, current mirror OTAs were used. Though the architecture for both OTAs is the same, the sizing of the transistors is different for each stage. The transistors for stage 1 are drawn larger than those for stage 2 to reduce input-referred 1/*f* noise. The differential pairs in each OTA operate in weak inversion.

Each OTA is biased with dc currents provided by a programmable bias generator. MOS switches and binary-weighted polysilicon resistors are used to create a programmable resistor in each bias generator. Commands from off chip set the resistance of the bias generator. The bias current sets the transconductance of each OTA. This in turn changes the high cutoff frequency of the ECoG amplifier. Therefore the current can be tuned to give the bandwidth needed for a given signal, over a range of 80 – 240 Hz.

B. Analog Multiplexer Design

On-chip reference voltages set the dc level of each ECoG amplifier output to 1.0V. With the amplifier gain of 60 dB, an input signal swinging from -1 mV to +1 mV produces an output voltage swing from 0 V to 2 V. Since the amplifier array shares a single ADC through an analog multiplexer, the output of each amplifier needs to be fast enough for the worst-case scenario in which an amplifier has to change the ADC's input by 2 V. All 100 amplifiers are connected to a common multiplexer output line that runs across the entire chip. This global node has a relatively high capacitance: 3 pF. The slew rate of each amplifier must be high enough to support the ADC sampling rate of 15.7 kS/s, which is shared across 32 channels. (Each channel is sampled at 490 S/s.) If we used a traditional OTA with a fixed bias current as an output buffer, the bias current of this OTA (which would be repeated in all 100 amplifiers on the chip) would need to be at least 3 mA to provide sufficient slew rate on the 3 pF MUX output line. To avoid the excessive static power consumption produced by this approach, we instead implemented a local buffer using an adaptive bias amplfier first presented in [4]. The schematic of the adaptive bias buffer is shown in Fig. 4. Transistor sizes used in this amplifier (when implemented in a 0.6-µm process) are listed in Table I.

At its heart the adaptive bias amplifier is a current mirror OTA, similar to the amplifiers used for the gain stages. Added to the classic OTA are two current subtractors. The current subtractors take the difference of the current through the branches of the differential pair. The drain currents from M_{21} and M_{20} are then fed to the input differential pair, effectively increasing the bias current when there is a significant difference between the drain currents in the differential pair. There will be a difference in the differential pair current only when the buffer's bias current is not great enough to keep the input and output voltages the same. Thus the adaptive bias op-amp will use more power only when it needs to be faster than its quiescent current will allow it to be. This architecture achieves the worst-case slew rate while limiting the static and average-case power dissipation to acceptable levels.

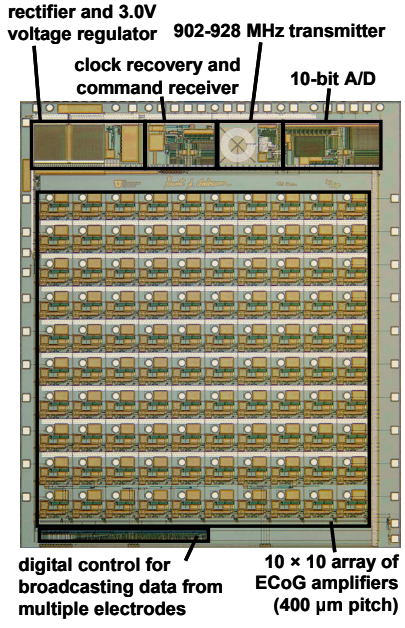

Figure 2. Microphotograph of 5.4 × 4.7 mm^2 INI-E wireless ECoG recording chip, fabricated in a commercial 0.6-µm 2P3M BiCMOS process

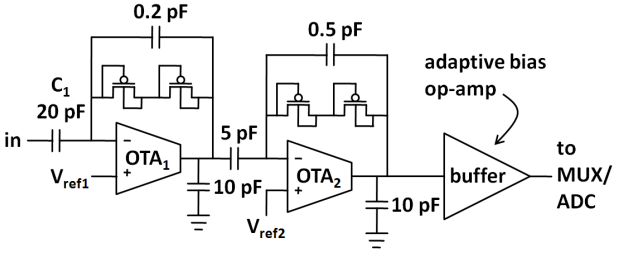

Figure 3. Three-stage ECoG amplifier.

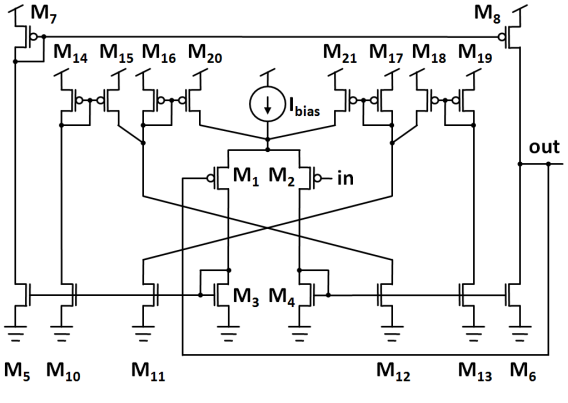

Figure 4. Circuit diagram of adaptive bias op-amp configured as a buffer.

TABLE I. ADAPTIVE BIAS AMP DEVICE SIZES

Transistors	W/L (µm/µm)
$M_1 - M_2$	20.0 / 0.6
$M_3 - M_6$	6.0 / 1.2
$M_7 - M_8$	12.0 / 1.2
$M_{10} - M_{13}$	6.0 / 1.2
$M_{14} - M_{19}$	16.2 / 4.0
$M_{20} - M_{21}$	32.4 / 4.0

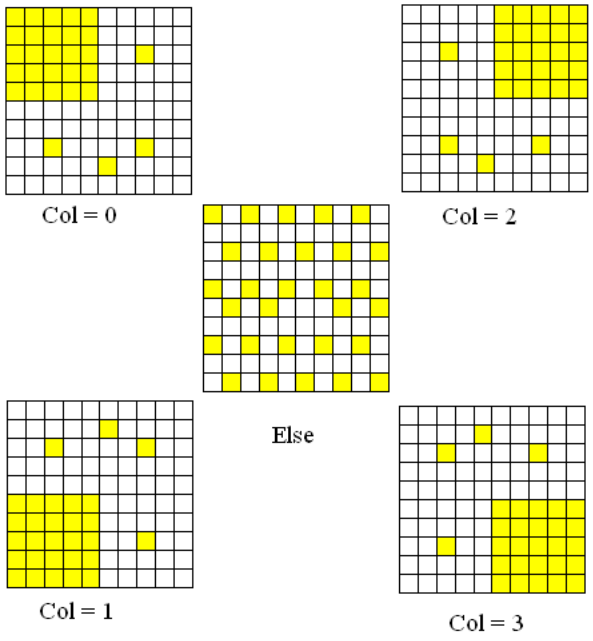

Figure 5. Five preset patterns of 29 electrodes selectable through the on-chip control logic.

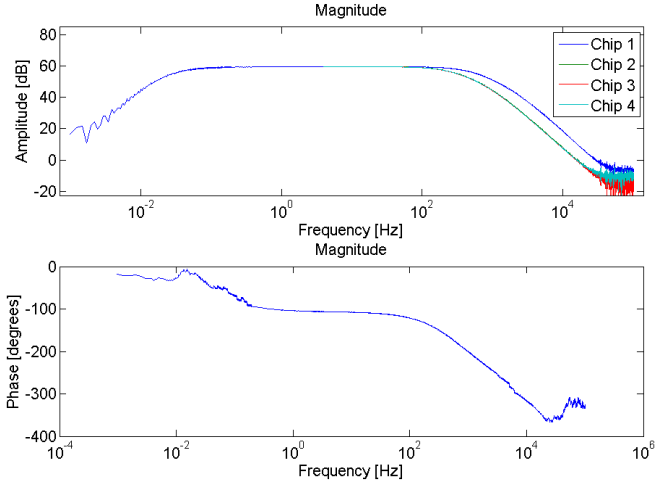

Figure 6. Top: Measured gain transfer functions of four measured ECoG amplifiers. Bottom: Measured phase transfer function from one of the ECog amplifiers.

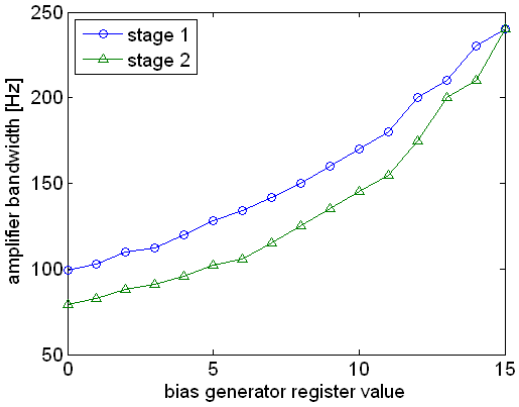

Figure 7. On-chip 4-bit registers are used to program the bandwidth of the ECoG amplifier stages.

C. *Control Logic*

To transmit data wirelessly, the ADC is connected to a frequency-shift-keying (FSK) RF transmitter [2]. To send multiple ECoG signals off chip, a digital control unit was designed to multiplex a selected subset of amplifiers through the single ADC. There are five user-selectable pre-programmed patterns that can be cycled through. Each subset pattern consists of 29 ECoG amplifiers from the 10 x 10 array and the three on-chip voltage and temperature sensors (see Fig. 5). The logic is made up of four basic logic blocks: a multiplexer, select logic to control the multiplexer, a five bit counter, and next-state logic.

III. EXPERIMENTAL RESULTS

A. *Characterization of the Amplifier*

Fabricated chips were tested while being powered and controlled wirelessly over an inductive link. Fig. 6 shows the measured transfer functions of four ECoG amplifiers measured from four different chips with their bias registers set for maximum bandwidth (i.e., 240 Hz). For all other tests, the bandwidth of each amplifier was limited to extend from 0.05 Hz to 200 Hz. Fig. 7 shows the measured 3-dB high-frequency cutoff of the first and second amplifier stages in response to the programmable bias generators that provide dc current to the OTAs. The bandwidth of each amplifier stage may be tuned to account for fabrication variations, and to accommodate particular ECoG signals of interest.

Amplifier noise originates from two sources: noise inherent in the amplifier, and noise injected from the power supply due to finite amplifier power supply rejection ratio (PSRR). The PSRR of the amplifiers was measured to be 42 dB at midband. While this is a relatively modest value for PSRR, an on-chip voltage regulator helps to create a quiet supply voltage from the ac inductive power link. Over the bandwidth of the ECoG amplifiers, the regulated power supply has a measured noise level of 260 μV_{rms} during wireless powering. The amplifier itself has an inherent input-referred noise of 2.8 μV_{rms}. Combined, these two noise sources yield a total input-referred noise of 3.5 μV_{rms} during wireless inductive powering of the chip. Fig. 8 shows the measured noise spectrum from the output of an amplifier.

B. *Test of Wireless Operation and Multiplexing*

To test the digital control logic, a sine wave of 10 Hz was applied to one of the 100 on-chip ECoG amplifiers and a triangle wave of 60 Hz was applied to a second amplifier. The chip was then sent a command to cycle through the pattern that included both these electrodes (see Fig. 5). The received signal from the on-chip ADC was converted back to an analog voltage using a DAC, and connected to the oscilloscope. Fig. 9 shows 200 ms of data as the on-chip MUX switches through 29 different amplifiers and three auxiliary sensors. The red and green lines show the ADC samples that correspond to the two active amplifiers connected to the 10 Hz sine wave and 60 Hz triangle wave. DC voltages from an on-chip voltage sensor and temperature sensors are also labeled. This experiment demonstrates that the digital control logic is working as designed, and is capable of interleaving data from multiple electrodes, permitting real-time monitoring of 29 ECoG channels.

IV. Conclusions

The entire 100-amplifier chip consumes 7.2 mW of power, making it safe for cortical implantation [5]. Another amplifier suitable for ECoG recording was previously reported in [6]. Perhaps the biggest limitation of the INI-E chip is the number of electrodes that it can wirelessly transmit data from continuously. As shown in [1], the spatial resolution of ECoG signals is finer than once believed, so more electrodes can be used for a given cortical region. Telemetry capable of supporting higher data rates must be implemented to permit wireless ECoG recording from 100 or more electrodes.

Acknowledgment

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References

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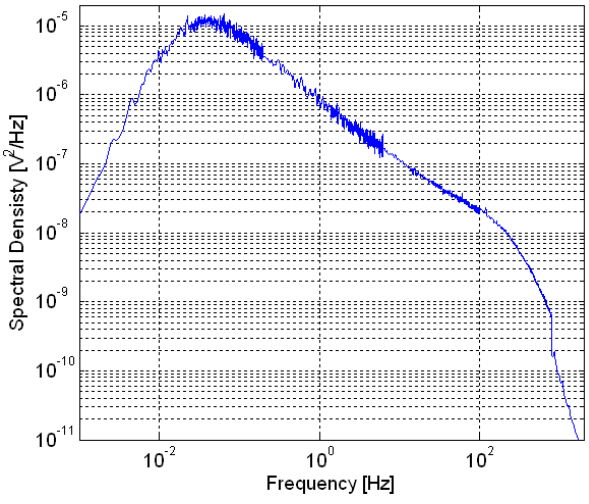

Figure 8. Measured noise spectral density at the output of an ECoG amplifier.

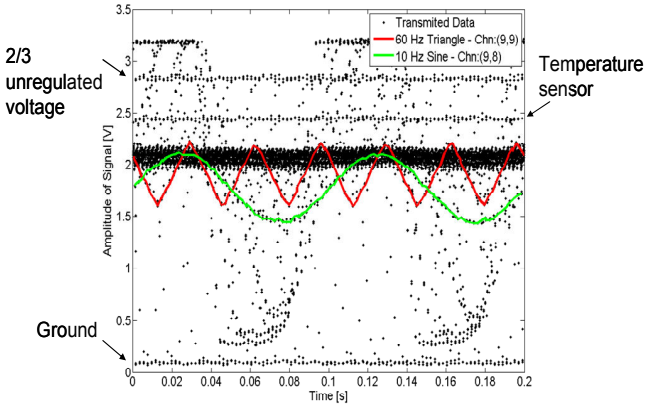

Figure 9. Wireless transmitted interleaved data with five of the multiplexed signals annotated.